What is claimed is:

1. A layout design system of a semiconductor integrated circuit, comprising:

a library information storage unit configured to register a basic via shape list;

a technology database storage unit configured to register a list expressing an optimum wire terminating process for each via shape of said basic via shape list registered in said library information storage unit; and

a central processing control unit configured to refer to the lists respectively registered in said library information storage unit and said technology database storage unit, select an optimum line processing, and execute a line design.

2. The layout design system of claim 1, wherein said central processing control unit configured to be constituted by a plurality of processing control sub-units.

3. The layout design system of claim 1, wherein said central processing control unit includes:

a layout design module configured to prepare a list expressing said optimum line processing by referring to the list registered in said library information storage unit, register the list in said technology database storage unit, and execute a layout processing;

a line processing module configured to refer to the list registered in the technology database storage unit and perform the line processing; and

an optimum via selection module configured to select an optimum via during processing by said line processing module.

4. A computer implemented layout design method, comprising:

preparing a basic via shape list and registering the basic via shape list in a library information storage unit;

referring to said basic via shape list registered in said library information storage unit, preparing a list expressing an optimum wire terminating process for each via shape of said basic via shape list, and registering the list in a technology database storage unit;

referring to the list registered in said technology database storage unit, and selecting an optimum line processing to perform the selected line processing; and

selecting an optimum via.

5. The computer implemented layout design method of claim 4, wherein said selecting said via, includes:

selecting a via applicable to all of said wire terminating processs; and

selecting a via most suitable for each of said wire terminating processs when the via applicable to all of said wire terminating processs can not be selected in said selecting said via.

6. A line design program for allowing a computer to execute, comprising:

preparing a basic via shape list, and registering the basic

via shape list in a library information storage unit;

referring to said basic via shape list registered in said library information storage unit, preparing a list expressing an optimum wire terminating process for each via shape of said basic via shape list, and registering the list in a technology database storage unit;

referring to the list registered in said technology database storage unit, and selecting an optimum line processing to perform the selected line processing; and

selecting an optimum via.

7. The line design program of claim 6, wherein the procedure for selecting said via, includes:

selecting a via applicable to all of said wire terminating processs; and

selecting a via most suitable for each of said wire terminating processs when the via applicable to all of said wire terminating processs can not be selected in said selecting said via.

8. A computer implemented layout design method, comprising:

generating a first line having a first line width and extending in a predetermined direction;

generating a second line having a second line width, extending in a direction different from said first line, and having its terminal end overlapping a terminal end of said first line;

stretching said first line in a longitudinal direction thereof;

stretching said second line in a longitudinal direction thereof by a length 1/2 times as long as the second line width;

deleting a projection from the terminal end of said first line and the terminal end of said second line, the projection protruding from an overlapped area where the terminal end of said first line and the terminal end of said second line overlap; and

setting a connection pattern having a polygon connecting said first and second lines at an intersection point of a longitudinal center line of said first line and a longitudinal center line of said second line.

9. The layout design method of claim 8, wherein said first and second lines are lines generated in different levels.

10. The layout design method of claim 8, wherein said first and second lines are lines generated in the same level.

11. The layout design method of claim 8, wherein said polygon is octagonal.

12. The layout design method of claim 11, wherein said first and second lines are lines generated in different levels.

13. The layout design method of claim 11, wherein said first and second lines are lines generated in the same level.

14. The layout design method of claim 8, wherein in said stretching

said first line in the longitudinal direction thereof, said first line is stretched by a length 1/2 times as long as the line width of said second line.

15. The layout design method of claim 8, wherein in said stretching said second line in the longitudinal direction thereof, said second line is stretched by a length 1/2 times as long as the line width of said first line.

16. A manufacturing method of a semiconductor integrated circuit, comprising:

forming a first line extending in a predetermined direction on a semiconductor substrate;

forming a level interlayer insulating film on said first line;

forming a polygon via hole penetrating through said level interlayer insulating film;

forming a connection conductive portion filling said polygon via hole and connecting with said first line; and

forming a second line extending at an angle unperpendicularly relative to said first line and having a terminal end connected to said connection conductive portion.